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Electronic Version v1.1

Stylesheet Version v1.1.0

Title of Invention

A METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR
GENERATING AND VERIFYING ISOLATION LOGIC MODULES IN DESIGN
OF INTEGRATED CIRCUITS

Application Number :

Date :

First Named Applicant: Bhanu KAPOOR

Confirmation Number:

Attorney Docket Number: Q82851

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Documents being submitted:	Files
us-fee-sheet	Q82851-usfees.xml us-fee-sheet.xsl us-fee-sheet.dtd
us-ids	Q82851-usidst.xml us-ids.dtd us-ids.xsl
us-request	Q82851-usrequ.xml us-request.dtd us-request.xsl
us-assignment	Q82851-usassn.xml us-assignment.xsl us-assignment.dtd Q82851asg.tif
us-declaration	Q82851dec1.tif
us-declaration	Q82851dec2.tif
application-body	ABX1.xml application-body.dtd Image1.tif Image2.tif Image3.tif Image4.tif Image5.tif Image6.tif Image7.tif Image8.tif Image9.tif isoamsa.ent isoamsb.ent isoamsc.ent isoamsn.ent isoamso.ent isoamsr.ent isobox.ent isocyr1.ent isocyr2.ent isodia.ent isogr1.ent isogr2.ent isogr3.ent isogr4.ent isolat1.ent isolat2.ent isomfrk.ent isomopf.ent isomscr.ent isonum.ent isopub.ent isotech.ent mathml2.dtd

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